PATENT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS & INTERFERENCES

Applicant:	FOO ET AL.	)	Examiner V. Kovalick
Appl. No.	10/647,723	)	Art Unit 2629
Confirm. No.	2166	)	Atty. Docket No. CS22497RA
Filed:	25 August 2003	)	

Title: "Matrix Display Having Addressable Display Elements And Methods"

APPEAL BRIEF UNDER 37 C.F.R. 41.37(c)

Assistant Commissioner for Patents
Alexandria, Virginia 22313

Sir:

Real Party In Interest

The real party in interest is Motorola Inc., by virtue of an assignment duly executed by the named inventor(s) and recorded in the Patent Office.

Related Appeals & Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1-5, 7-17, 19 and 20 are pending. Claims 6 and 18 have been canceled. The pending claims are reproduced in Appendix A.

Claims 5, 7-9, 17, 19 and 20 are allowed. Claims 2, 3 and 13-15 were indicated as being allowable but stand objected to for dependence on rejected base or intermediate claims.

Claims 1, 4, 10-12 and 16 are rejected and are the subject of the instant appeal.

Status of Amendments

The claims have not been amended subsequent to the mailing of the final Office Action on 20 March 2007.

Summary of Claimed Subject Matter

Claim 1 is drawn to a method of activating a display element in a display device having n x m array of display elements, wherein each display element coupled to a logic controlled switch. Page 4, line 7- page 7, line 20. The method comprises applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element, applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element, and activating the display element with the logic controlled switch when the row address and

row electrode inputs and when the column address and column electrode inputs satisfy a condition. Page 4, line 9 – page 6, lines 12 & FIGS. 4-6.

Claim 10 is drawn to a display device comprising a plurality of display elements arranged in a matrix, each display element includes a display pixel coupled to a switch and an addressable latch having an output coupled to a controlling input of the switch, wherein the addressable latch having a row address input and a column address input. Page 4, line 7- page 7, line 20 & FIGS. 4-6.

Grounds of Rejection for Review on Appeal

Whether Claims 1, 10-11 and 16 are patentable over U.S. Publication 2002/0210363 (Yasukawa) under 35 USC 103(a).

Whether Claim 4 is patentable over Yasukawa in view of U.S. Publication No. 2003/0020671 (Santoro) under 35 USC 103(a).

Whether Claim 12 is patentable over Yasukawa in view of U.S. Patent No. 6,094,704 (Martin) under 35 USC 103(a).

Arguments re: Yasukawa

Rejection Summary

Claims 1, 10-11 and 16 stand rejected under 35 USC 103(a) as being unpatentable over U.S. Publication 2002/0210363 (Yasukawa).

Discussion of Claim 1

Regarding Claim 1, Yasukawa fails to disclose or suggest a

> ... method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:
>
> applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;
>
> applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;
>
> activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Yasukawa discloses reducing flickering and degradation of image quality caused by stray light in a TFT switched display by forming a light shield over a channel region of each TFT. Yasukawa also connects a capacitor (70) in parallel with each TFT to reduce leakage of the image signal.

The Examiner's assertion that what is described in Claim 10 is a general description of what is disclosed by Yasukawa is not supported by the prior art. According to Claim 1, four (4) inputs are applied to the logic controlled switch: row address and electrode inputs, and column address and electrode inputs. The Examiner's action does not expressly address the row and column electrode limitations of Claim 1. Nevertheless, contrary to the Examiner's assertion, the scanning line (3a) and the data line (6a) inputs to the TFT (30) of Yasukawa do not and cannot read on the limitations of Claim 1. The TFT (30) of Yasukawa includes only two inputs. Claim 1 is thus patentabley distinguished over Yasukawa.

Discussion of Claim 10

Regarding Claim 10, Yasukawa fails to disclose or suggest a

> … display device comprising:
> a plurality of display elements arranged in a matrix,
> each display element including a display pixel coupled to a switch,
> each display element including an addressable latch having an output coupled to a controlling input of the switch,
> the addressable latch having a row address input and a column address input.

Yasukawa discloses reducing flickering and degradation of image quality caused by stray light in a TFT switched display by forming a light shield over a channel region of each TFT. Yasukawa also connects a capacitor (70) in parallel with each TFT to reduce leakage of the image signal.

The Examiner's assertion that what is described in Claim 10 is a general description of what is disclosed by Yasukawa is not supported by the prior art. According to the Examiner, the pixel electrode (9a) of Yasukawa corresponds to the claimed "display element". Contrary to the Examiner's assertion, however, Yasukawa does not disclose elements corresponding to the "switch" and the "addressable latch" of Claim 10. The TFT (30) of Yasukawa cannot correspond to both the "switch" and the "addressable latch" of Claim 10. Claim 10 requires that the "addressable latch" include "an output coupled to a controlling input of the switch". Yasukawa does not disclose this structure. Claim 10 is thus patentabley distinguished over Yasukawa.

Discussion of Claim 11

Regarding Claim 11, Yasukawa fails to disclose or suggest in combination with Claim 11 an "...addressable latch having a row electrode input and a column electrode input." According to Claim 11, four (4) the addressable latch includes four (4) inputs: row address and electrode inputs, and column address and electrode inputs. Contrary to the Examiner's assertion, the scanning line (3a) and the data line (6a) inputs to the TFT (30) of Yasukawa do not and cannot read on the limitations of Claim 11. The TFT (30) of Yasukawa includes only two inputs. Claim 11 is thus further patentably distinguished over Yasukawa.

Arguments re: Yasukawa & Santoro

Rejection Summary

Claim 4 stands rejected under 35 USC 103(a) as being unpatentable over Yasukawa in view of U.S. Publication 2003/0020671 (Santoro).

Discussion of Claim 11

Regarding Claim 4, Yasukawa and Santoro fail to disclose or suggest in combination with Claim 1

> ... activating at least some display elements of the display device at a first refresh rate,

activating other display elements of the display device at a second refresh rate, different than the first refresh rate.

Claim 4 is allowable over the putative combination of Yasukawa and Santoro for at least the reasons set forth in Claim 1. Further, contrary to the Examiner's assertion, there is no suggestion in the prior art to combine Yasukawa with Santoro in the manner claimed. Santoro suffers from at least the same deficiencies of Yasukawa. Moreover, one of ordinary skill would not be motivated to combine the teachings of a silicon architect like Yasukawa concerned with reducing flickering, stray light and leakage in a TFT switched display with the teaching of a software engineer like Santoro concerned with developing an improved user interface. Claim 4 is thus further patentably distinguished over Yasukawa and Santoro.

Arguments re: Yasukawa & Martin

Rejection Summary

Claim 12 stands rejected under 35 USC 103(a) as being unpatentable over Yasukawa in view of U.S. Patent 6,094,704 (Martin).

Discussion of Claim 11

Regarding Claim 12, Yasukawa and Martin fail to disclose or suggest in combination with Claim 10

> ... the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch,
>
> the row address input coupled to the row address logic, the column address input coupled to the column address logic.

Martin discloses a high speed memory device with pipelined row and column address paths, which is unrelated to the subject matter of Claims 10-12 and 16. One of ordinary skill would not be motivated to combine the teachings of a silicon architect like Yasukawa concerned with reducing flickering, stray light and leakage in a TFT switched display with the teaching of an architect of high speed memory devices. Claim 12 is thus further patentably distinguished over Yasukawa and Martin.

Prayer For Relief

In view of the discussion above, all Claims of the present application are in condition for allowance. Kindly withdraw any rejections and allow this application to issue as a United States Patent without delay.

Respectfully submitted,

/ ROLAND K. BOWLER II/

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ROLAND K. BOWLER II 25 JUL. 2007
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Claims Appendix

1. (Original) A method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:

applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;

applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;

activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

2. (Previously Presented) The method of Claim 1,

comparing the row address input and the row electrode input,

comparing the column address input and the column electrode input,

activating the display element with the logic controlled switch based on results of the comparisons.

3. (Original) The method of Claim 2, controlling the logic-controlled switch includes enabling and disabling the logic controlled switch with a charging capacitor.

4. (Original) The method of Claim 1,

activating at least some display elements of the display device at a first refresh rate,

activating other display elements of the display device at a second refresh rate, different than the first refresh rate.

5. (Previously Presented) A method in a display device comprising an n x m array of addressable display elements, the method comprising:

activating at least some display elements characterizing a foreground image at a first rate;

activating other display elements characterizing a background image at a second rate,

the second rate less than the first rate;

activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Claim 6 (Canceled).

7. (Previously Presented) The method of Claim 5,

comparing the row address input and the row electrode input,

comparing the column address input and the column electrode input,

activating the display element with the logic controlled display element switch using the results of the comparisons.

8. (Previously Presented) The method of Claim 7, enabling and disabling the logic controlled display element switch with a switch enabling charging capacitor controlled by the results of the comparisons.

9. (Original) The method of Claim 5, activating other display elements at the second rate includes not activating the other display elements.

10. (Original) A display device comprising:

a plurality of display elements arranged in a matrix,

each display element including a display pixel coupled to a switch,

each display element including an addressable latch having an output coupled to a controlling input of the switch,

the addressable latch having a row address input and a column address input.

11. (Original) The device of Claim 10, the addressable latch having a row electrode input and a column electrode input.

12. (Original) The device of Claim 10,

the addressable latch of each display element including row address logic and column address logic having corresponding outputs coupled to the output of the addressable latch,

the row address input coupled to the row address logic, the column address input coupled to the column address logic.

13. (Original) The device of Claim 10,

the addressable latch of each display element including first and second comparators, the first comparator having the row address input and a row electrode input, the second comparator having the column address input and a column electrode input,

each display element including a logic device having a first input coupled to an output of the corresponding first comparator, the logic device having a second input coupled to an output of the corresponding second comparator.

14. (Original) The device of Claim 13, the logic device is an AND gate, the output of the addressable latch is an output the logic device

15. (Original) The device of Claim 13, a pixel capacitor connected parallel with the display pixel, and a switch enabling capacitor coupled to an input of the switch.

16. (Original) The device of Claim 10 is a thin-film-transistor display device.

17. (Previously Presented) A method in a display device comprising an n x m array of addressable display elements, the method comprising:

selectively activating display elements by individually addressing the display elements to be activated, activating the display elements includes,

applying a row address input and a row electrode input to control logic of the corresponding display element,

applying a column address input and a column electrode input to the control logic of the corresponding display element, and

activating the display element with a logic controlled switch when the control logic inputs satisfy a condition;

reducing power consumption by addressing at least some of the display elements at a first frequency and addressing other display elements at a second frequency, the second frequency less than the first frequency.

Claim 18 (Canceled).

19. (Previously Presented) The method of Claim 17,

comparing the row address input and the row electrode input with the control logic,

comparing the column address input and the column electrode input with the control logic,

activating the display element by enabling the logic controlled switch using the results of the comparisons.

20. (Original) The method of Claim 19, enabling and disabling the logic controlled switch with a switch enabling capacitor controlled by the control logic.

Evidence Appendix

(None)

Related Proceedings Appendix

(None)